Lab 5: Sequential Circuit Analysis

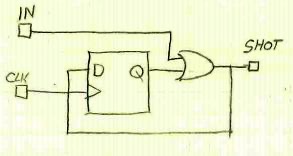
**Primary Objectives:**

1. Get experience analyzing simple sequential logic circuits implemented with D-type positive edge triggered flip-flops.
2. Get experience building and testing the given simple sequential logic circuits in Logisim.

**Circuit 1**

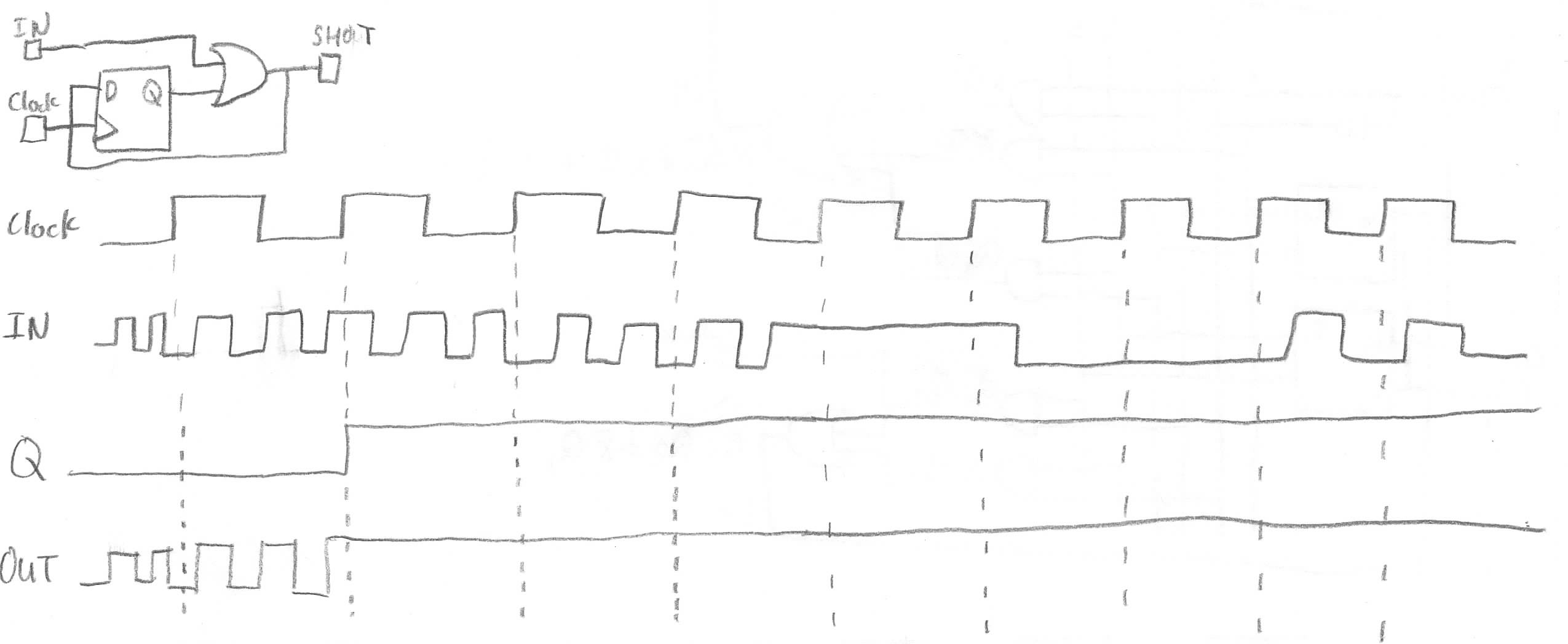
**Given Circuit**

Figure 1: The first given circuit that requires analysis



**Functional Timing Diagram**

Figure 2: A functional timing diagram for the first circuit with a randomized input



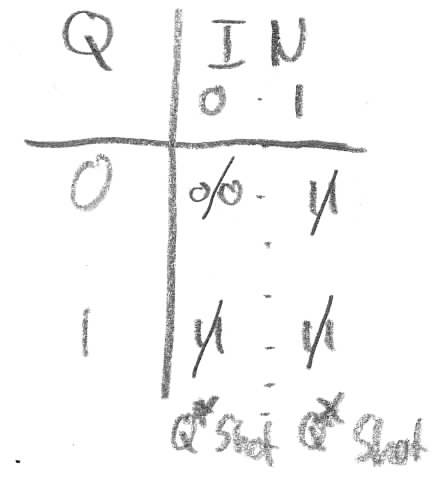
The functional timing diagram shows that the output turns on while the input is on, but output only remains on once the D-type flip flop’s clock turns on while the input is on.

**Logic Equations, State Table, and State Diagram**

SHOT = IN + Q

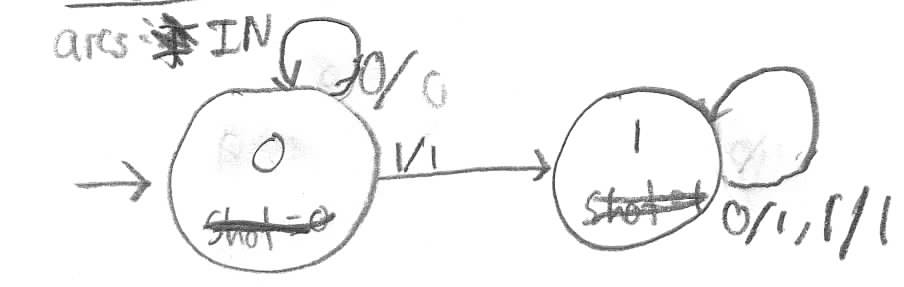
D = IN + Q

Table 1: The state table for the first circuit



As seen in the state table, the first circuit is a mealy device. This means both the next state and the output are dependent on the input.

Figure 3: The State Diagram for the first circuit



The state diagram reflects the states shown in the state table.

**Comments:** The inclusion of a clock as an input in this circuit has necessarily complicated the analysis of this circuit as both previous and current states must be tracked.

**Implementation**

Figure 4: The first circuit implemented in Logisim



The circuit as seen in Figure 1 implemented in Logisim

Table 2: Logging of the first circuit implemented in Logisim

|  |  |  |  |
| --- | --- | --- | --- |
| IN | Clock(50,70) | Q0 | SHOT |
| 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 |

The table is consistent with the state diagram seen in figure 3

**Timing Information**

Setup Time (input to output) = DFF setup + AND-2 max = 10ns + 3ns = 13ns

Hold Time (input to output) = DFF hold – AND-2 min = 4ns – 1ns = 3ns

Propagation Delay clock to output (min) = DFF min + AND-2 min = 7ns + 1ns = 8ns

Propagation Delay clock to output (max) = DFF max + AND-2 max = 9ns + 3ns = 12ns

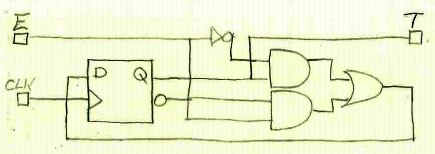
Max Clock Rate = 1/ (DFF max + DFF setup + AND-2 max) = 1/(9ns + 10ns + 3ns) = 1/(22ns)

Note: Propagation Delay input to output could be calculated for this device since it is a mealy device; however, that information was not requested and as such it will not be provided.

**Circuit 2**

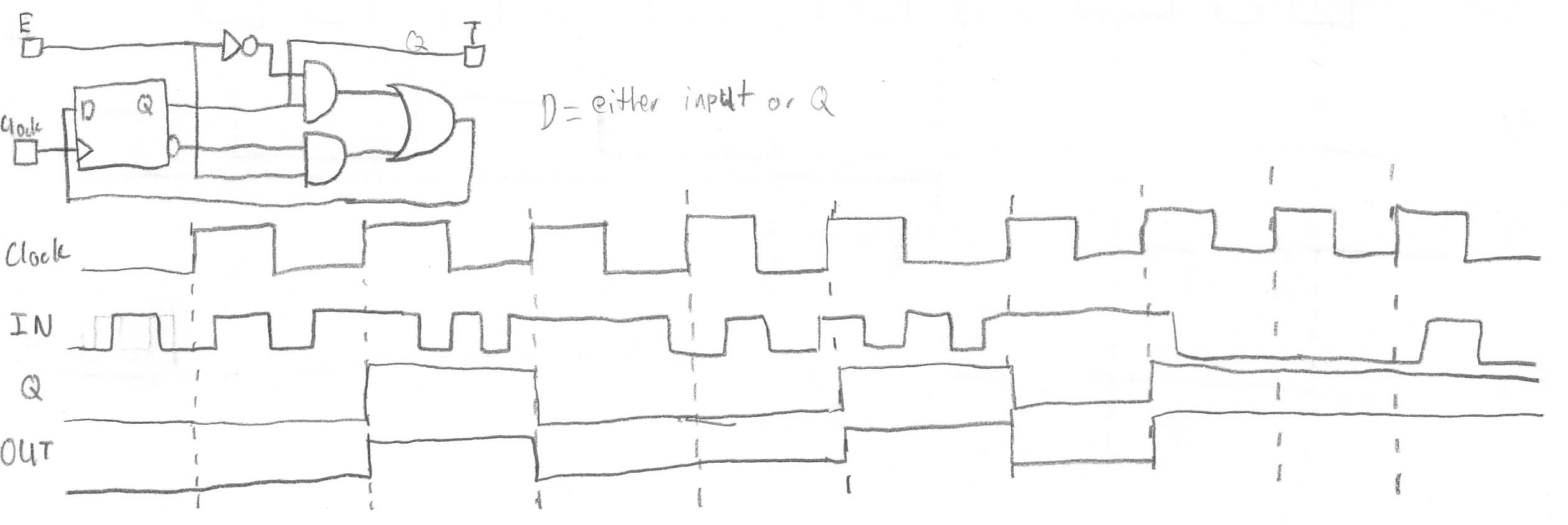
**Given Circuit**

Figure 5: The second given circuit that requires analysis



**Functional Timing Diagram**

Figure 6: A functional timing diagram for the second circuit with a randomized input

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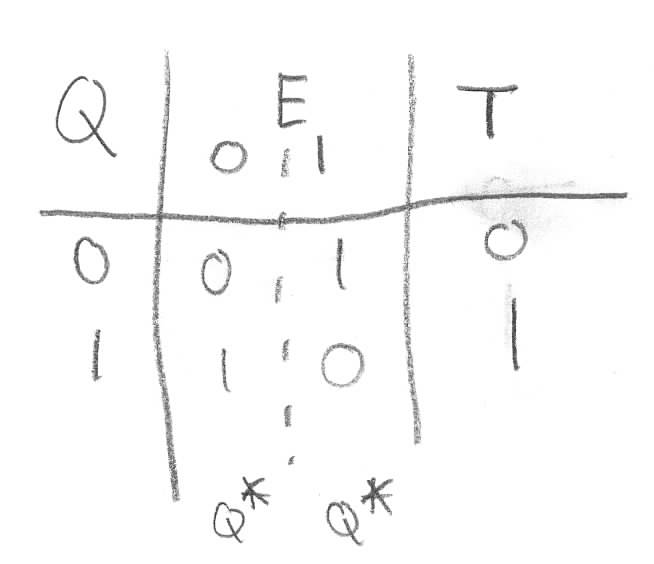
The functional timing diagram shows that the output is the same as Q from the D-type flip flop, and that Q will remain/turn on when either E or the D-type flip flop is on during a clock tick.

**Logic Equations, State Table, and State Diagram**

T = Q

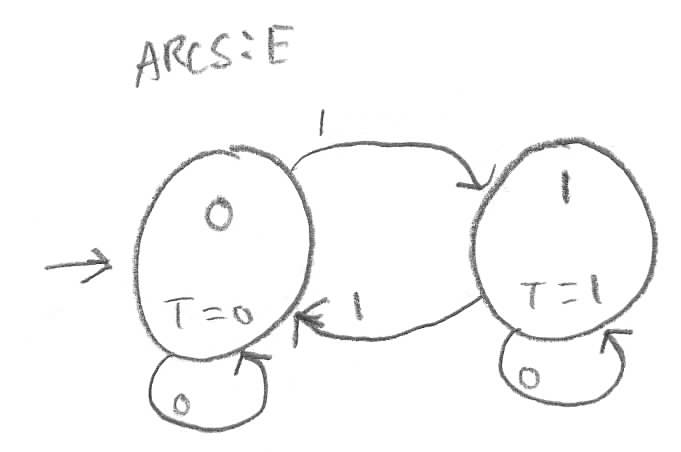
D = E’Q + EQ’

Table 3: The state table for the second circuit



As seen in the state table above, the second circuit is a Moore device. This means the output is not directly dependent on the input.

Figure 7: The state diagram for the second circuit



The state diagram reflects the states shown in the state table.

**Comments:** The inclusion of a clock as an input in this circuit has necessarily complicated the analysis of this circuit as both previous and current states must be tracked.

**Implementation**

Figure 8: The second circuit implemented in Logisim



The circuit as seen in Figure 5 implemented in Logisim

Table 4: Logging of the second circuit implemented in Logisim

|  |  |  |  |
| --- | --- | --- | --- |
| E | Clock(40,70) | Q0 | T |
| 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 |

The table is consistent with the state diagram seen in figure 6

**Timing Information**

Setup Time (input to output) = DFF setup + (INV-1 max + AND-2 max + OR-2 max)

= 10ns + (2ns + 3ns + 3ns) = 18ns

Hold Time (input to output) = DFF hold – (AND-2 min + OR-2 min)

= 4ns – (1ns + 1ns) = 2ns

Propagation Delay clock to output (min) = DFF min + (AND-2 min + OR-2 min)

= 7ns + (1ns + 1ns) = 9ns

Propagation Delay clock to output (max) = DFF max + (INV-1 max + AND-2 max + OR-2 max)

= 9ns + (2ns + 3ns + 3ns) = 17ns

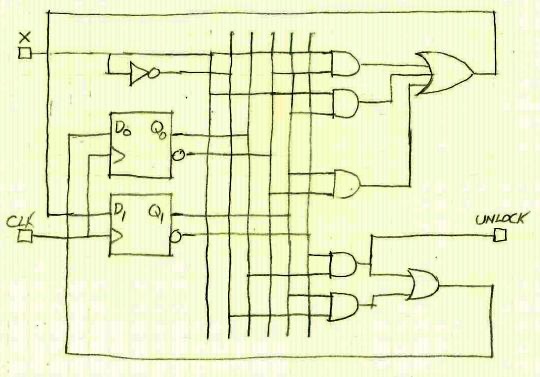
Max Clock Rate = 1/ (DFF max + DFF setup + (INV-1 max + AND-2 max + OR-2 max))

= 1/(9ns + 10ns + (2ns + 3ns + 3ns)) = 1/(27ns)

**Circuit 3**

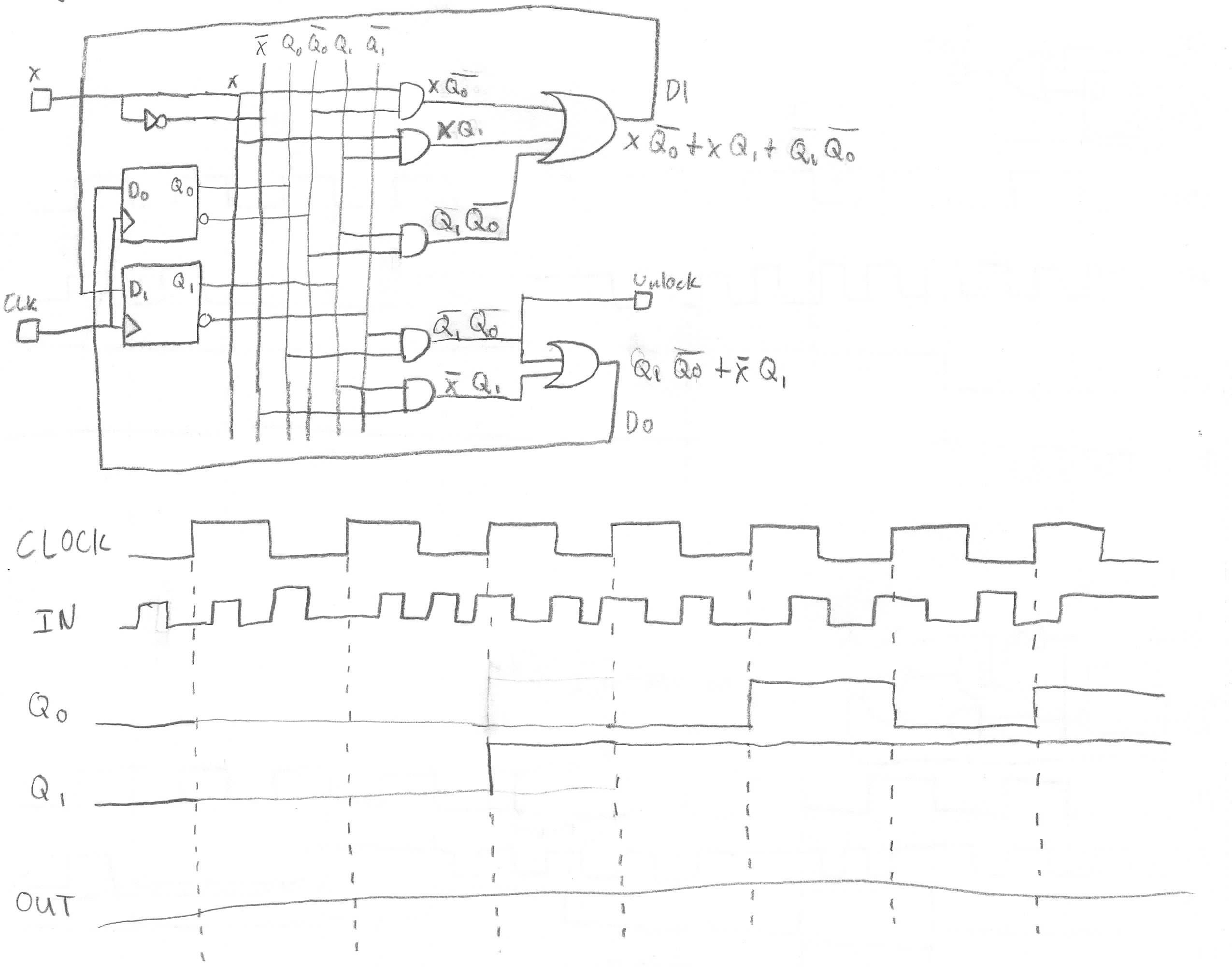
**Given Circuit**

Figure 9: The third given circuit that requires analysis



**Functional Timing Diagram**

Figure 10: A functional timing diagram for the third circuit with a randomized input



This functional timing diagram failed to reach any meaningful conclusions relating input to output, as such discussion on what this circuit does will be discussed later in the report.

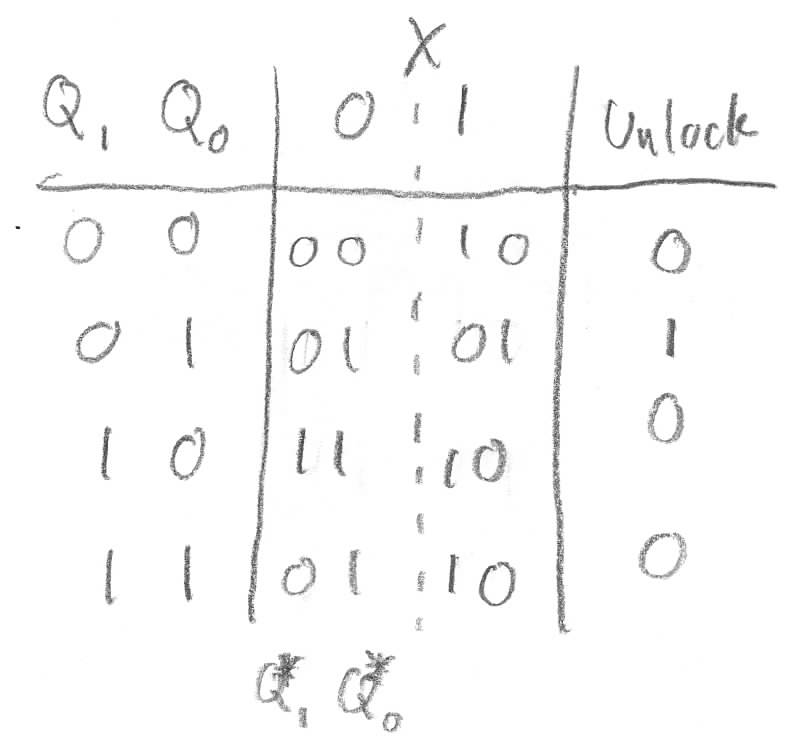
**Logic Equations, State Table, and State Diagram**

Unlock = Q1’Q0

D1 = xQ0’ + xQ1 + Q1Q0’

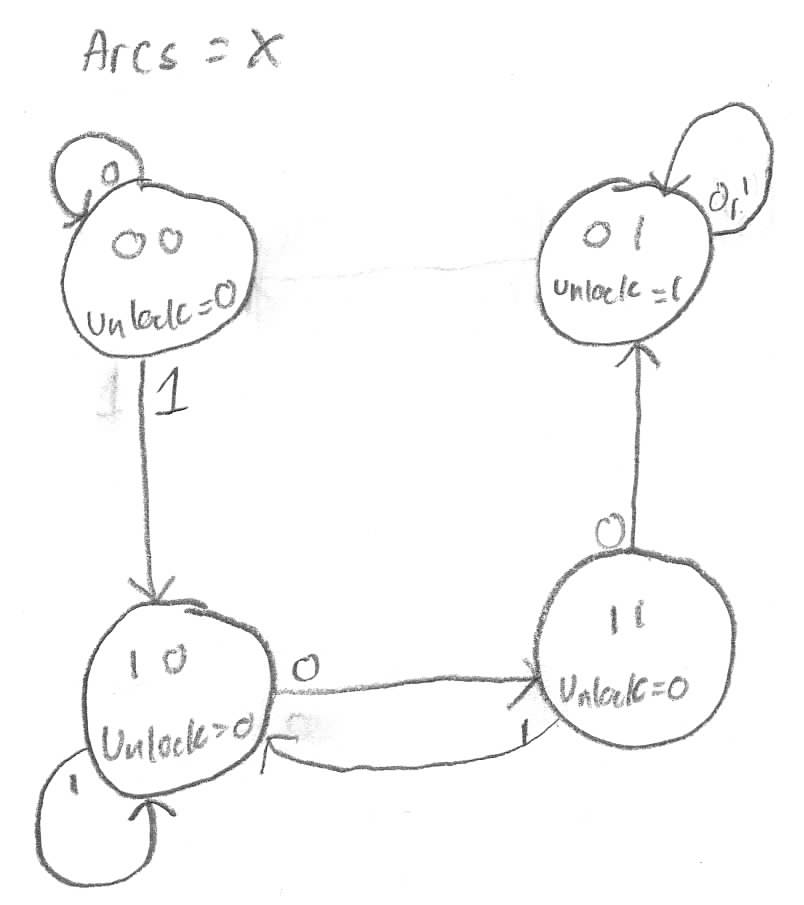
D0 = Q1Q0’ + x’Q1

Table 5: The state table for the third circuit



As seen in the state table above, the second circuit is a Moore device. This means the output is not directly dependent on the input.

Figure 11: The state diagram for the third circuit



The state diagram reflects the states shown in the state table. The state table also describes the function of the circuit as a circuit that requires the input 1 followed by 00 to unlock, which could not be seen in the functional timing diagram due to the randomized input frequently changing between 1 and 0 during every clock tick.

**Comments:** The inclusion of a clock as an input in this circuit has necessarily complicated the analysis of this circuit as both previous and current states must be tracked.

**Implementation**

Figure 12: The third circuit implemented in Logisim



The circuit as seen in Figure 9 implemented in Logisim

Table 6: Logging of the third circuit implemented in Logisim

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| X | Clock(40,170) | Q1 | Q0 | UNLOCK |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 |

The table is consistent with the state diagram seen in figure 11

**Timing Information**

Setup Time (input to output) = DFF setup + (AND-2 max + OR-3 max)

= 10ns + (3ns + 6ns) = 19ns

Hold Time (input to output) = DFF hold – (AND-2 min + OR-2 min)

= 4ns – (1ns + 1ns) = 2ns

Propagation Delay clock to output (min) = DFF min + (AND-2 min + OR-2 min)

= 7ns + (1ns + 1ns) = 9ns

Propagation Delay clock to output (max) = DFF max + (AND-2 max + OR-3 max)

= 9ns + (3ns + 6ns) = 18ns

Max Clock Rate = 1/ (DFF max + DFF setup + (AND-2 max + OR-3 max))

= 1/(9ns + 10ns + (3ns + 6ns)) = 1/(28ns)

**Conclusion**

Experience analyzing simple sequential logic circuits implemented with D-type positive edge triggered flip-flops has been gained, and the circuits work as expected.